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10/608,575	06/30/2003	Tae Yun Kim	40296-0006	7309

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EXAMINER	
TSAI, SHENG JEN	
ART UNIT	**PAPER NUMBER**
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,575	KIM, TAE YUN	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *3-5 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,7,12,14,19 and 21-23* is/are rejected.

7)☒ Claim(s) *8-11,13 and 15-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicants' Amendment and Remarks filed on July 26, 2006 regarding application 10/608,575 filed on June 30, 2003.

2. Claims 1, 6 and 10-11 have been amended.

Claims 3-5 and 20 have been cancelled previously.

Claims 1-2, 6-19 and 21-23 are pending for consideration.

3. ***Response to Amendments and Remarks***

Applicants' amendments and remarks have been fully and carefully considered, with the Examiner's response set forth below.

Independent claim 1 has been amended to include the new limitation of "... **selectively activating a quarter or a half of a plurality of the banks and a quarter or a half of the activated banks depending on states of the plurality of control signals when a refresh operation signal is activated.**"

Applicant contends that the prior art (Hwang et al., US 6,590,822) does not teach or suggest this newly recited limitation. The Examiner disagrees with this assessment for the following reasons:

First, Hwang et al. do teach "selectively activating a quarter or a half of the activated banks depending on states of the plurality of control signals when a refresh operation signal is activated" [More specifically, the present invention provides mechanisms for performing a PASR operation for, e.g., 1/2, 1/4, 1/8, or 1/16 of a selected memory bank (column 2, lines 50-57); column 13, lines 4-25; column 13, lines 43-59; column 15, lines 50-60].

Second, Hwang et al. do teach "selectively activating a quarter or a half of a plurality of the banks depending on states of the plurality of control signals when a refresh operation signal is activated" [**column 10, lines 32-45** describe the case where only bank 1 is selected for refresh operation while the refresh operation is not performed on bank 2 through bank 4; **column 11, lines 69-67** and **column 12, lines 1-3** describe the case where only bank 1 and bank 2 are selected for refresh operation while the refresh operation is not performed on bank 3 and bank 4; **column 12, lines 4-15** describe the case where only bank 1, bank 2 and bank 3 are selected for refresh operation while the refresh operation is not performed on bank 4; and **column 12, lines 16-23** describe the case where all 4 banks are selected for refresh operation]. Thus, Hwang et al. indeed teach selectively activating a quarter (i.e., one out of four banks) or a half (two out of four banks) of a plurality (four) of the banks.

Therefore, the Examiner's position regarding the patentability of all claims remains the same as stated in the previous Office Action.

Another iteration of claim analysis based on the reference relied on previously (Hwang et al., US 6,590,822) has been embarked. Refer to the corresponding sections of the claim analysis for details.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-2, 6-7, 12, 14, 19 and 21-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Hwang et al. (US 6,590,822).

As to claim 1, Hwang et al. disclose **a self-refresh device** [System and method for Performing Partial Array Self-Refresh Operation in a Semiconductor Memory Device (title)], **comprising**:

a command decoder for decoding an externally inputted refresh command to output a mode register set signal, a self-refresh signal and a refresh flag signal [the memory device enters into a self-refresh mode in response to an externally input command signal (column 2, lines 11-23); the command buffer, figure 16, 1601; column 13, lines 60-67; column 14, lines 1-4; The refresh entry detector 207 includes an entry detecting part 301, a latching part 303 and a termination detecting part 305. The entry detecting part 301 detects the entry into a self-refresh mode by means of an internal clock signal PCLK, a first internal clock enable signal PCKE1, a chip selection signal/CS, a column address strobe signal/GAS and a write enable signal/WE. In other works, if a semiconductor memory device enters into a self-refresh mode, the output signal N302 of the entry detecting part 301 makes a transition to a logic "high" state (column 7, lines 25-42)];

a refresh counter for performing a counting operation corresponding to a refresh cycle in response to the refresh flag signal to output a refresh request signal [cell

data are amplified in connection with a self-refresh counter in Block1, figure 15a (column 17, lines 1-7)];

an internal address counter for counting and generating an internal address in response to the refresh flag signal and the refresh request signal [figure 16, 1605, shows the internal address counters; column 2, lines 57-65];

a partial array self-refresh decoder [abstract; column 2, lines 50-57] **for generating a plurality of control signals for performing a partial array self-refresh operation in response to the mode register set signal, the self-refresh signal, and the internal address** [a mode register setting signal PMRS is at a logic high level ... (column 8, lines 27-48); column 3, lines 13-31]; **and**

a row address strobe generator [RAS, figure 4; column 7, lines 60-67] **for generating a row active signal** [RCON1 and RCON2, column 10, lines 50-55] **for selectively activating a quarter or a half of a plurality of the banks** [column 10, lines 32-45 describe the case where only bank 1 is selected for refresh operation while the refresh operation is not performed on bank 2 through bank 4; column 11, lines 69-67 and column 12, lines 1-3 describe the case where only bank 1 and bank 2 are selected for refresh operation while the refresh operation is not performed on bank 3 and bank 4; column 12, lines 4-15 describe the case where only bank 1, bank 2 and bank 3 are selected for refresh operation while the refresh operation is not performed on bank 4; and column 12, lines 16-23 describe the case where all 4 banks are selected for refresh operation. Thus, Hwang et al. indeed teach selectively activating a quarter (i.e., one out of four banks) or a half (two out of four banks) of a plurality (four)

of the banks] **and a quarter or a half of the activated banks** [More specifically, the present invention provides mechanisms for performing a PASR operation for, e.g., 1/2, 1/4, 1/8, or 1/16 of a selected memory bank (column 2, lines 50-57); column 13, lines 4-25; column 13, lines 43-59; column 15, lines 50-60] **depending on states of the plurality of control signals when a refresh operation signal is activated** [column 3, lines 5-12; column 10, lines 32-45; column 11, lines 69-67 and column 12, lines 1-3; column 12, lines 4-15; column 12, lines 16-23].

As to claim 2, Hwang et al. teach that **the device according to claim 1, further comprising:**

a row pre-decoder for outputting an external address as a row address in a normal mode, and outputting the internal address as the row address in a refresh mode [the row address pre-decoder, figure 16, 1607; column 3, lines 45-50].

As to claim 6, Hwang et al. teach that **the device according to claim 1, wherein the partial array self-refresh decoder comprises**:

an extended mode register set decoder for outputting a register set control signal by decoding a bank selection address in response to the mode register set signal [a mode register setting signal PMRS is at a logic high level ... (column 8, lines 27-48)];

a plurality of address latches each of which for outputting register set addresses by latching an external address, in response to the register set control signal, the self-refresh signal, and the mode register set signal [column 8, lines 3-18];

and

a partial array self-refresh controller for selectively activating the plurality of control signals by decoding the plurality of register set addresses depending on input of the internal address [the refresh controller, figure 2, 217; column 6, lines 39-45].

As to claim 7, Hwang et al. teach that **the device according to claim 6, wherein the register set control signal is activated when the mode register set signal is activated, a most significant bit address of the bank selection address is high, and a second most significant bit of the bank selection address is low** [a mode register setting signal PMRS is at a logic high level ... (column 8, lines 27-48)].

As to claim 12, Hwang et al. teach that **the partial array self-refresh controller outputs the plurality of control signals by decoding the plurality of register set addresses and the plurality of inverted register set addresses** [abstract; column 2, lines 50-57; a mode register setting signal PMRS is at a logic high level ... (column 8, lines 27-48); column 3, lines 13-31].

As to claim 14, Hwang et al. teach that **the device according to claim 1, wherein the row address strobe generator generates the row active signal depending on a bank selection address and a normal operation signal in a normal mode, and generates the row active signal depending on the plurality of control signals and the refresh operation signal activated in a refresh mode** [during a normal operating mode ..., column 2, lines 1-10; column 6, lines 10-22; column 8, lines 3-17].

As to claim 19, Hwang et al. teach that **the row address strobe generator is comprised to have the same number of the banks** [figure 16; column 3, lines 5-12].

As to claim 20, refer to "As to claim 1."

As to claim 21, Hwang et al. teach that **the extended mode register set decoder sets up a code for performing a self-refresh operation on a cell array corresponding to a half of one bank when a partial array self-refresh operation is in a half of bank mode, and for performing a self-refresh operation on a cell array corresponding to a quarter of one bank when a partial array self-refresh operation is in a quarter of bank mode** [1/2, 1/4, 1/8 or 1/16 of a selected memory bank (column 2, lines 50-57)].

As to claim 22, Hwang et al. teach that **when the partial array self-refresh operation is in a half of bank mode, the partial array self-refresh decoder activates a number of control signals corresponding to a quarter of the plurality of control signals until a most significant bit of address becomes high** [1/2, 1/4, 1/8 or 1/16 of a selected memory bank (column 2, lines 50-57)].

As to claim 23, Hwang et al. teach that **when the partial array self-refresh operation is in a quarter of bank mode, the partial array self-refresh decoder activates a number of control signals corresponding to a quarter of the plurality of control signals until at least one of two most significant bits of address becomes high** [1/2, 1/4, 1/8 or 1/16 of a selected memory bank (column 2, lines 50-57)].

Allowable Subject Matter

6. Claims 8-11, 13 and 15-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. ***Related Prior Art of Record***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Tsern et al., (US 6,345,009), "Apparatus and Method for Refreshing Subsets of Memory Devices in a Memory System."
- Jung, (US 6,137,742), "Semiconductor Memory Device Having Self-Refresh Control Circuit."
- Seyyedy, (US 5,818,777), "Circuit for Implementing and Method for Initiating Slef-Refresh Mode."

Conclusion

8. Claims 1-2, 6-7, 12, 14 and 19-23 are rejected as explained above.

Claims 8-11, 13 and 15-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

August 4, 2006

PIERRE BATAILLE
PRIMARY EXAMINER

8/4/06